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The performance evaluation of a 3D torus network using partial link-sharing method in NoC router buffer (Article)

Fukase, N.[a] ✉, Miura, Y.[a], Watanabe, S.[a], Rahman, M.M.H.[b]

[a]Graduate School of Technology, Shonan Institute of Technology, SIT, Fujisawa-shi, Japan
[b]Dept. of Computer Science, KICT, International Islamic University, Malaysia

Abstract

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The high performance network-on-chip (NoC) router using minimal hardware resources to minimize the layout area is very essential for NoC design. In this paper, we have proposed a memory sharing method of a wormhole routed NoC architecture to alleviate the area overhead of a NoC router. In the proposed method, a memory is shared by multiple physical links by using a multi-port memory. In this paper, we have proposed a partial link-sharing method and evaluated the communication performance using the proposed method. It is revealed that the resulted communication performance by the proposed methods is higher than that of the conventional method, and the progress ratio of the 3D-torus network is higher than that of 2D-torus network. It is shown that the improvement of communication performance using partial link sharing method is achieved with slightly increase of hardware cost.
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Interconnection network Multiport memory Network-on-chip (NoC) Router

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